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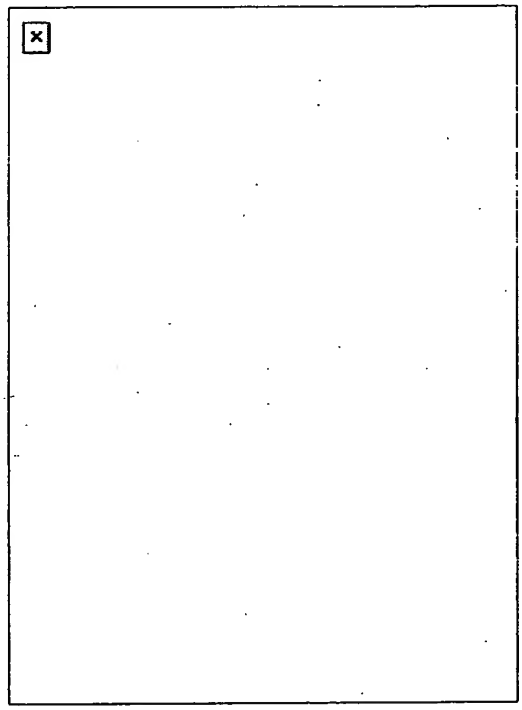
(54) CIRCUIT AND METHOD FOR SCAN TEST

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a scan test circuit in which the number of test pins required for a scan test of an LSI is reduced to a minimum and which reduces the testing time.

SOLUTION: The scan test circuit is provided with a shift register 11 and a shift register 12 which constitute two scan chains, to which a scan-in signal IN1, a scan clock CLK and a scan enable signal EN are supplied and which output a scan-out signal OUT1 and a scan-out signal OUT2, an inverter 2 which inverts the clock CLK and which outputs an inversed clock BCK, a selector 3 which responds to the supply of the enable signal EN, and selects one from among the clock CLK and the inversed clock BCK and which outputs a selected clock CKS so as to be supplied to the shift register 12, and a selector 41 which is synchronized with the clock CLK and which selects one from among the scan-out signals OUT1, OUT2 at the shift registers 11, 12 so as to be output as a scan-out signal SCO1.



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* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the scanning test circuit and the scanning test approach for testing the logical circuit of a logical circuit LSI (semiconductor integrated circuit) about a scanning test circuit and the scanning test approach.
[0002]
[Description of the Prior Art] Conventionally, in the logical circuit LSI which especially consists of a combinational circuit, it has inside LSI the scanning test circuit which is a test specialized circuit for the formation of test easy of a circuit function, and what checks that the combinational circuit is operating normally is widely used by carrying out the test by the scanning pass method.
[0003] This scanning test circuit consists of scanning pass circuit chains which connected the scanning pass flip-flop to the serial, and operates as a shift register so that it may be well-known. This scanning test circuit has the scanning test input terminal which inputs the scanning test signal which is data for a scanning test (scanning test pattern) from the exterior or the interior of LSI, the scanning clock terminal which inputs the clock for a scanning pass test from the exterior of LSI, and the scanning test output terminal to which the scanning test output data which they are as a result of a scanning test are outputted.
[0004] A scanning pass method inputs the scanning test pattern for a test from a scanning test input terminal at the time of a static test mode (shift mode). Carry out and the scanning clock for a test is inputted into a clock terminal. (Following and scan in) Carry out logical operation of the data by the combinational circuit inside LSI, and the predetermined expected value which is the result of an operation as scanning test output data From a scanning test output terminal to an output (The following, scan-out) By checking being carried out, it checks that the combinational circuit is operating normally. That is, if it is as the expected value which scanning test output data calculated beforehand, there will be no defect in a combinational circuit, and if it is not as expected value, it will judge with there being poor manufacture.
[0005] Thus, by adopting a scanning test circuit, the interior of a circuit can be separated as a combination circuit, and a test becomes easy. In order to set up and read data to the scanning chain by which scanning connection was made, the number of clocks is required by the number of a scanning register. Since the number of clocks required for a test increases that the number of scanning chains is one, the number of clocks required in order to set up and read data to a scanning register by making a scanning chain into plurality can be decreased. Moreover, although there are a scanning in pin which inputs the test enabling pin which carves test actuation and normal operation, and scanning data, and a scan-out pin which outputs scanning data in the external terminal (pin) which needs to be added for a scanning design, a scanning in pin and a scan-out pin can be made to use also [pin / of a general logical circuit / the data input / output pin].

[0006] That is, the more there are many scanning chain numbers, since it decreases, the number of flip-flops, i.e., number of necessary clocks, per scanning chain, the time amount spent on a scanning inn / scan-out becomes short, and, the more test cost decreases.
[0007] However, the number of terminals (the following, pin) of LSI has become settled for every type of LSI, therefore the pin usable as a scanning in pin / a scan-out pin is restricted physically. Moreover, when the data input / output pin of a general logical circuit are used also [pin / a scanning in pin / / scan-out], since a general logical circuit is influenced of the time delay increase by scanning chain addition etc., it cannot necessarily increase the number of scanning chains unconditionally. Furthermore, the number of scanning test datas in which an input/output is possible may have a limit from constraint of a circuit tester at coincidence. In recent years, the semiconductor integrated circuit is large-scale-ized and necessary test time amount is also increasing. Therefore, reduction of test durations is an important technical problem.
[0008] The conventional scanning test circuit can be classified into the following two construction from a viewpoint of the number of test pins, and the number of test patterns.
[0009] The 1st conventional scanning test circuit by the 1st construction divides into plurality the scanning chain which constitutes a scanning test circuit, and prepares a scanning in pin and a scan-out pin for each [which was divided] scanning chain of every.
[0010] For example, the 2nd conventional scanning test circuit by the 2nd construction given in JP,1-217278,A The decoder which outputs the selection signal which a scanning control signal input pin is connected for reduction of the number of test pins, and chooses one of two or more of the scanning chains, The demultiplexer which inputs the scanning in pin signal of each shift register of two or more scanning chains single to any one according to the selection signal which this decoder outputs, It has a multiplexer for outputting any one output of the above-mentioned shift register to a scan-out pin single as a scan-out signal according to the above-mentioned selection signal. Sequential selection of either of the shift registers is made using the above-mentioned decoder, a demultiplexer, and a multiplexer.
[0011] When drawing 5 which shows the 1st conventional scanning test circuit with a block is referred to, this 1st conventional scanning test circuit The scanning in pin which constitutes each scanning chain divided into two or more (this example 3) books, and each of the scanning in signals IN1, IN2, and IN3 inputs, The scanning clock pin which the scanning clock CLK inputs, It has the shift registers 51, 52, and 53 which have the scan-out pin which outputs each of the scanning enabling pin which the scanning enable signal EN inputs, and the scan-out signals OUT1, OUT2, and OUT3, respectively.
[0012] Next, probably, if actuation of the 1st conventional scanning test circuit, i.e., the 1st conventional scanning test approach, is explained with reference to drawing 6 which shows drawing 5 and the wave of each signal by the timing diagram, since the scanning enable signal EN is "L" in time of day T1, even if it receives supply of the scanning clock CLK, shift registers 51, 52, and 53 will not operate.
[0013] Next, the scanning enable signal EN becomes "H" at time of day T2, and scanning actuation is started. the rising edge of the scanning clock CLK -- synchronizing -- each data of the scanning in signals IN1, IN2, and IN3 -- A2, A3, and A4 ..., B-2, B3, and B4 ..., and C2, C3 and C4 -- it changes with ... A shift register 51 reads the data A2 of the scanning in signal IN1, A3, and A4, and outputs the scanning result data D1, D2, and D3 which perform a shift action and correspond inside as a scan-out signal OUT1. Similarly, a shift register 52 reads data B-2 of the scanning in signal IN2, B3, and B4, performs a shift action inside, and outputs the scanning result data E1, E2, and E3 as a scan-out signal OUT2. Similarly, a shift register 53 reads the data C2, C3, and C4 of the scanning in signal IN3, and a shift action performs it inside, and it outputs the scanning result data F1, F2, and F3 as a scan-out signal OUT3.
[0014] When drawing 7 which shows the 2nd conventional scanning test circuit with a block is

referred to, this 2nd conventional scanning test circuit The scanning in pin which constitutes each of the scanning chain of two or more (this example 3) books, and each of the scanning in signals IN1, IN2, and IN3 inputs, The shift registers 61, 62, and 63 which have the scan-out pin which outputs each of the scanning clock pin which the scanning clock CLK inputs, the scanning control pin which the scanning enable signal EN inputs, and the scan-out signals SO1, SO2, and SO3, respectively, The decoder 64 which outputs the selection signal SL which decodes according to supply of the scanning control signal CS, and chooses one of shift registers 61, 62, and 63, and the scanning enable signal EN of the selected shift register, The demultiplexer 65 which chooses and outputs one of the scanning in signals IN1, IN2, and IN3 according to a selection signal SL, It has the multiplexer 66 which chooses one of each scan-out signals SO1, SO2, and SO3 of shift registers 61, 62, and 63 according to a selection signal SL, and is outputted as a scan-out signal SCO.

[0015] Next, drawing 8 which shows drawing 7 and the wave of each signal by the timing diagram is referred to. If actuation of the 2nd conventional scanning test circuit, i.e., the 2nd conventional scanning test approach, is explained, it will set at time of day T1 first. Since the scanning control signal CS is "0", the selection signal SL and each scanning enable signals EN1, EN2, and EN3 of an output of a decoder 65 are altogether set to "L", and even if it receives supply of the scanning clock CLK, shift registers 61, 62, and 63 do not operate. In addition, in the expedient top of illustration, and drawing 7 , the scanning enable signals EN1, EN2, and EN3 are displayed with one signal line.

[0016] Next, the scanning control signal CS is set to "1" at time of day T2, and a decoder 65 makes scanning actuation start by making only the scanning enable signal EN1 of a shift register 61 into "H". At this time, since the scanning enable signals EN2 and EN3 of shift registers 62 and 63 are "L", these shift registers 62 and 63 do not operate. Synchronizing with the rising edge of the scanning clock CLK, the data J1 of the scanning in signal IN1 are sent to the shift register 61 chosen by the demultiplexer 65. A shift register 61 reads data J1, performs a shift action inside, performs logical operation and supplies it to a multiplexer 66 by making the corresponding, scanning result data P1 into the scan-out signal SO 1. A multiplexer 66 outputs the scan-out signal [P1] SO 1, i.e., scanning result data, as a scan-out signal SCO.

[0017] When a shift register 61 finishes scanning by the data J1 of the scanning in signal IN1, the scanning control signal CS is set to "2", and a decoder 65 makes scanning actuation start by making only the scanning enable signal EN2 of a shift register 62 into "H". At this time, since the scanning enable signals EN1 and EN3 of shift registers 61 and 63 are "L", these CIF TOREJITASU 61 and 63 does not operate. Synchronizing with the rising edge of the scanning clock CLK, the data K1 of the scanning in signal IN2 are sent to the shift register 62 chosen by the demultiplexer 65. A shift register 62 reads data K1, and supplies the scanning result data Q1 which perform a shift action and logical operation and correspond inside to a multiplexer 66. A multiplexer 66 outputs the scan-out signal [Q1] SO 2, i.e., scanning result data, as a scan-out signal SCO.

[0018] When a shift register 62 finishes scanning by the data K1 of the scanning in signal IN2, the scanning control signal CS is set to "3", and a decoder 65 makes scanning actuation start by making only the scanning enable signal EN3 of a shift register 63 into "H". At this time, shift registers 61 and 62 answer "L" of each scanning enable signals EN1 and EN2, and do not operate. Synchronizing with the rising edge of the scanning clock CLK, the data L1 of the scanning in signal IN3 are sent to the shift register 63 chosen by the demultiplexer 65. A shift register 63 reads data L1, and supplies the scanning result data R1 which perform a shift action and logical operation and correspond inside to a multiplexer 66. A multiplexer 66 outputs the scan-out signal [R1] SO 3, i.e., scanning result data, as a scan-out signal SCO.

[0019] When a shift register 63 finishes scanning by the data L1 of the scanning in signal IN3, the scanning control signal CS is set to "1", and a decoder 65 makes scanning actuation start

by making only the scanning enable signal EN1 of a shift register 61 into "H".
[0020] The above actuation is repeated.
[0021] although the number of test patterns can be reduced, since a scanning in pin and a scan-out pin are needed for every each of two or more shift registers, it has the trouble that the number of necessary test pins will increase, so that the number of the scanning test circuit [conventional / 1st] of shift registers, i.e., a scanning chain, increases.
[0022] Moreover, although the 2nd conventional scanning test circuit can do the number of test pins few, in order that it may test for every selected shift register, It is necessary to repeat the same test several same times with the number of shift registers, and to perform it. No shift registers, i.e., scanning chains, could be tested to coincidence, but it had the trouble of taking after all test time amount comparable as the case where carry out series connection of all the shift registers as one scanning chain, and they are tested.
[0023]
[Problem(s) to be Solved by the Invention] although the number of test patterns could be reduced, since the scanning in pin and the scan-out pin were needed for every each of two or more shift registers, they had the fault that the number of necessary test pins will increase, so that the number of the approach [1st / conventional test circuit / scanning / and conventional scanning test approach] which were mentioned above of shift registers, i.e., a scanning chain, increased.
[0024] Moreover, although the 2nd conventional scanning test circuit can reduce the number of test pins, since it needs to test for every selected shift register, It is necessary to repeat the same test several same times with the number of shift registers, and to perform it. No shift registers, i.e., scanning chains, could be tested to coincidence, but there was a fault of it being said after all that it will take test time amount comparable as the case where carry out series connection of all the shift registers as one scanning chain, and they are tested.
[0025] The purpose of this invention is to offer the scanning test circuit and the scanning test approach of reducing test time amount while it solves the above-mentioned fault and holds down the number of necessary test pins to the scanning test of LSI to the minimum.
[0026]
[Means for Solving the Problem] The scanning test circuit of invention according to claim 1 It has the scanning chain which consists of series-connection circuits of two or more flip-flops for testing the internal circuitry of LSI which consists of a logical circuit, and is operated as a shift register. The scanning test data and the scanning clock for a test are inputted at the time of a static test mode. In the scanning test circuit which tests the scanning pass method which checks that carry out logical operation by said internal circuitry, and said internal circuitry is carrying out normal actuation based on the scan-out result data which are the output of the result of an operation Said 1st shift register which operates synchronizing with the 1st edge of said scanning clock, Said 2nd shift register which operates synchronizing with the 2nd edge of said scanning clock, It has an output change means to change the 1st and 2nd scan-out data which is each output of said 1st and 2nd shift registers, and to output said scan-out result data, and is constituted.
[0027] Moreover, in a scanning test circuit according to claim 1, said 1st edge is a rising edge and invention according to claim 2 is characterized by said 2nd edge being a falling edge.
[0028] Moreover, invention according to claim 3 is equipped with the clock selector which answers supply of the inverter which reverses said scanning clock and outputs a reversal clock in a scanning test circuit according to claim 1, and the scanning enable signal which activates a scanning test circuit at the time of said static test mode, chooses either of said scanning clocks and said reversal clocks, outputs a selection clock, and is supplied to said 2nd shift register, and is constituted.
[0029] The scanning test circuit of invention according to claim 4 It has the scanning chain

which consists of series-connection circuits of two or more flip-flops for testing the internal circuitry of LSI which consists of a logical circuit, and is operated as a shift register. The scanning test data and the scanning clock for a test are inputted at the time of a static test mode. In the scanning test circuit which tests the scanning pass method which checks that carry out logical operation by said internal circuitry, and said internal circuitry is carrying out normal actuation based on the scan-out result data which are the output of the result of an operation The scanning in pin which constitutes each of the 1st and 2nd scanning chains, and a scanning in signal inputs, The scanning clock pin which said scanning clock inputs, The 1st and 2nd shift registers which have the scan-out pin which outputs each of the scanning enabling pin [which the scanning enable signal which activates a scanning test circuit inputs], 1st, and 2nd scan-out signals at the time of said static test mode, respectively, The inverter which reverses said scanning clock and outputs a reversal clock, The selector for a clocked into change which answers supply of said scanning enable signal, chooses either of said scanning clocks and said reversal clocks at the time of said static test mode, outputs a selection clock, and is supplied to said scanning clock pin of said 2nd shift register, It has the selector for an output change which chooses either of each and said 2nd scan-out signal of the 1st of said 1st and 2nd shift registers synchronizing with said scanning clock, and is outputted as said scan-out result data, and is constituted.

[0030] Moreover, invention according to claim 5 is set to a scanning test circuit according to claim 4. When said scanning enable signal is the 1st level, said selector for a clocked into change said scanning clock Said reversal clock is outputted as said selection clock, respectively at the time of the 2nd level. Said selector for an output change is characterized by outputting said 2nd scan-out signal for said 1st scan-out signal as said scan-out result data, respectively at the time of the 1st level, when said scanning clock is the 2nd level.

[0031] Moreover, invention according to claim 6 is set to a scanning test circuit according to claim 4. n flip-flops with which each of said 1st and 2nd shift registers is the latch holding the data whose each is 1 bit, and constitutes the shift register of n (positive integer) bit, Said scanning clock is supplied as a shift clock of said flip-flop at the time of said internal circuitry of m (positive integer) individual for a scanning test, and the activity level of said scanning enable signal. It has a clock mask means to carry out the mask of said scanning clock at the time of non-activity level, and to suspend supply of said shift clock, and is constituted.

[0032] Moreover, in the scanning test circuit according to claim 4, said clock mask means is equipped with the AND circuit which outputs the AND of said scanning enable signal and said scanning clock, and invention according to claim 7 is constituted.

[0033] The scanning test circuit of invention according to claim 8 It has the scanning chain which consists of series-connection circuits of two or more flip-flops for testing the internal circuitry of LSI which consists of a logical circuit, and is operated as a shift register. At the time of a static test mode, the scanning test data and the scanning clock for a test are inputted. In the scanning test circuit which tests the scanning pass method which checks that carry out logical operation by said internal circuitry, and said internal circuitry is carrying out normal actuation based on the scan-out result data which are the output of the result of an operation The scanning in pin which constitutes each of the 1st and 2nd scanning chains, and the 1st scanning in signal inputs, The scanning clock pin which said scanning clock inputs, The 1st and 2nd shift registers which have the scan-out pin which outputs each of the scanning enabling pin [which the scanning enable signal which activates a scanning test circuit inputs], 1st, and 2nd scan-out signals at the time of a static test mode, respectively, The scanning in pin which constitutes each of the 3rd and 4th scanning chains, and the 2nd scanning in signal inputs, The scanning clock pin which said scanning clock inputs, The 3rd and 4th shift registers which have the scan-out pin which outputs each of the scanning enabling pin [which the scanning enable signal which activates a scanning test circuit inputs], 2nd, and 3rd scan-out

signals at the time of said static test mode, respectively, The inverter which reverses said scanning clock and outputs a reversal clock, The selector for a clocked into change which answers supply of said scanning enable signal, chooses either of said scanning clocks and said reversal clocks at the time of said static test mode, outputs a selection clock, and is supplied to said scanning clock pin of said 2nd and 4th shift registers, The 1st selector for an output change which chooses either of each and said 2nd scan-out signal of the 1st of said 1st and 2nd shift registers synchronizing with said scanning clock, and is outputted as 1st scan-out result data, It has the 2nd selector for an output change which chooses either of each and said 4th scan-out signal of the 3rd of said 3rd and 4th shift registers synchronizing with said scanning clock, and is outputted as 2nd scan-out result data, and is constituted.

[0034] The scanning test approach of invention according to claim 9 is equipped with the scanning chain which consists of series-connection circuits of two or more flip-flops for testing the internal circuitry of LSI which consists of a logical circuit, and is operated as a shift register. The scanning test data and the scanning clock for a test are inputted at the time of a static test mode. In the test approach of a scanning pass method of checking carrying out logical operation by said internal circuitry, and said internal circuitry carrying out normal actuation based on the scan-out result data which are the output of the result of an operation Said 1st shift register is operated synchronizing with the 1st edge of said scanning clock. It is characterized by operating said 2nd shift register synchronizing with the 2nd edge of said scanning clock, changing the 1st and 2nd scan-out data which is each output of said 1st and 2nd shift registers, and outputting said scan-out result data.

[0035] Moreover, in the scanning test approach according to claim 9, said 1st edge is a rising edge and invention according to claim 10 is characterized by said 2nd edge being a falling edge.

[0036]

[Embodiment of the Invention] Next, the gestalt of operation of this invention is explained to a detail with reference to a drawing.

[0037] The scanning test circuit and the scanning test approach of a gestalt of this operation It has the scanning chain which consists of series-connection circuits of two or more flip-flops for testing the internal circuitry of LSI which consists of a logical circuit, and is operated as a shift register. The scanning test data and the scanning clock for a test are inputted at the time of a static test mode. In the scanning test circuit which tests the scanning pass method which checks that carry out logical operation by the above-mentioned internal circuitry, and said internal circuitry is carrying out normal actuation based on the scan-out result data which are the output of the result of an operation The 1st shift register which operates synchronizing with the 1st edge (starting) of the above-mentioned scanning clock, The 2nd shift register which operates synchronizing with the 2nd edge (falling) of the above-mentioned scanning clock, By having an output change means to change the 1st and 2nd scan-out data which is each output of the 1st and 2nd shift registers of the above, and to output scan-out result data It is characterized by operating to coincidence two scanning chains which are the 1st and 2nd shift registers of the above in both the rising edge of a scanning clock, and a falling edge.

[0038] If drawing 1 which shows the gestalt of operation of the 1st of this invention with a block is referred to, next, the scanning test circuit of the gestalt of this operation shown in this drawing The scanning in pin which constitutes each of two scanning chains and the scanning in signal IN1 inputs, The scanning clock pin which the scanning clock CLK inputs, The shift registers 11 and 12 which have the scan-out pin which outputs each of the scanning enabling pin which the scanning enable signal EN which activates a scanning test circuit inputs, and the scan-out signals OUT1 and OUT2 at the time of a static test mode, respectively, The inverter 2 which reverses the scanning clock CLK and outputs the reversal clock BCK, The selector 3 for a clocked into change which answers supply of the scanning enable signal EN, chooses either

of the scanning clock CLK and the reversal clock BCK, outputs the selection clock CKS, and is supplied to the scanning clock pin of a shift register 12, It has the selector 41 for an output change which chooses either of each scan-out signals OUT1 and OUT2 of shift registers 11 and 12 synchronizing with the scanning clock CLK, and is outputted as a scan-out signal SCO1.

[0039] With the gestalt of this operation, the selector 3 for the clocked into change of a shift register 12 outputs the scanning clock CLK, when the scanning enable signal EN is "L", and the reversal clock BCK is outputted as a selection clock CKS, respectively at the time of "H". Moreover, the selector 41 for an output change outputs the scan-out signal OUT1, when the scanning clock CLK is "H", and the scan-out signal OUT2 is outputted as a scan-out signal SCO1, respectively at the time of "L."

[0040] If drawing 2 which shows an example of the configuration of a shift register 11 with a block on behalf of shift registers 11 and 12 is referred to, the shift register 11 shown in this drawing F/F 111, 112, ..., 11n from which each is the latch (flip-flop) holding the data which are 1 bit, and constitutes the shift register of n (positive integer) bit, It has the internal circuitries 121, 122, ..., 12m of m (positive integer) individual for a scanning test, and AND circuit 131 which outputs the AND of the scanning enable signal EN and the scanning clock CLK as a shift clock CK.

[0041] The scanning enable signal EN carries out the mask of the scanning clock CLK at the period which is "L", and it is made, as for AND circuit 131, for a shift register 11 not to operate.

[0042] F/F [111, 112, ..., 11n] each outputs the value which holds the value of Input D by the rising edge of the shift clock CK, and is held from the output Q.

[0043] Although internal circuitries [121, 122, ..., 12m] each is a logical circuit based on the specification of a system and is considering as the black box here, it outputs the result of a meaning according to the condition of an input.

[0044] Next, if the gestalt scan test approach of actuation of the gestalt this operation, i.e., this operation, is explained with reference to drawing 3 which shows drawing 1 , drawing 2 , and the wave of each signal by the timing diagram, since supply of the shift clock CK has stopped with AND circuit 131 in time of day T1 first even if it receives supply of the scanning clock CLK, since the scanning enable signal EN is "L", shift registers 11 and 12 will not operate.

[0045] Next, since the scanning enable signal EN becomes "H", AND circuit 131 of a shift register 11 will be in a supply condition from the supply interruption condition of the shift clock CK and supply of the shift clock CK 1 is started by time-of-day T3, a shift register 11 starts scanning actuation. A selector 3 is supplied to it and coincidence at a shift register 12 by using as a scanning clock the reversal clock BCK which the inverter 2 reversed.

[0046] the timing of the rising edge of the scanning clock CLK -- synchronizing -- the scanning in signal IN1 --" of the scanning clock CLK -- the data S2 and S3 at the time of H", and S4 ... changing -- on the other hand -- the timing of a falling edge -- synchronizing -- the scanning in signal IN1 -- the data U2, U3, and U4 at the time of "L" of the scanning clock CLK -- it changes with ... Since it synchronizes with a rising edge, a shift register 11 reads the data S2 and S3 of the scanning in signal IN1, and S4, performs a shift action inside, performs logical operation and supplies it to a selector 41 by making the corresponding, scanning result data T1 and T2 and T3 into the scan-out signal OUT1.

[0047] Similarly, since it synchronizes with a falling edge, a shift register 12 reads the data U2, U3, and U4 of the scanning in signal IN1, performs a shift action inside, performs logical operation and supplies it to a selector 41 by making the corresponding, scanning result data V1, V2, and V3 into the scan-out signal OUT2.

[0048] Thus, since a shift register 11 and a shift register 12 output a separate result with a separate terminal (pin), a selector 41 is changed synchronizing with the rising edge and falling edge of the scanning clock CLK, the scan-out signal OUT1 is outputted at the time of a rising

edge, and the scan-out signal OUT2 is outputted as a scan-out signal SCO1, respectively at the time of a falling edge.

[0049] If the number of terminals usable as a scanning in pin / a scan-out pin of the scanning test circuit and the scanning test approach of a gestalt of this operation is equivalent as explained above, the number of scanning chains can be doubled substantially, therefore if the above-mentioned number of terminals and a clock frequency are equivalent, test time amount can be reduced in one half.

[0050] Next, when drawing 4 which shows the gestalt of operation of the 2nd of this invention with a block is referred to, the difference with the gestalt of the 1st operation of the above-mentioned of the gestalt of this operation shown in this drawing is having had 3 sets of scanning test circuits of the gestalt of the 1st operation, and having made the number of scanning chains into 3 times (6 [i.e.,]). Namely, the shift registers 11 and 12 of the gestalt of the 1st operation and AND circuit 2, The shift registers 13 and 14 which output each of the scan-out signals OUT3 and OUT4 according to supply of the scanning in signal IN2 in addition to a selector 3 and a selector 41, The shift registers 15 and 16 which output each of the scan-out signals OUT5 and OUT6 according to supply of the scanning in signal IN3, The selector 42 for an output change which chooses either of each scan-out signals OUT3 and OUT4 of shift registers 13 and 14 synchronizing with the scanning clock CLK, and is outputted as a scan-out signal SCO2, It is having the selector 43 for an output change which chooses either of each scan-out signals OUT5 and OUT6 of shift registers 15 and 16 synchronizing with the scanning clock CLK, and is outputted as a scan-out signal SCO3.

[0051] In addition to the gestalt of the 1st operation, and actuation of the shift register 11 which is an intersection, and 12 relation, the group of shift registers 13 and 14 and the group of shift registers 15 and 16 perform in parallel actuation which outputs each of the scan-out signals SCO2 and SCO3 in response to each supply of the scanning in signals IN2 and IN3, respectively, and also actuation of the gestalt of this operation is the same as that of the gestalt of the 1st operation.

[0052] As the Prior art explained, the duration of a scanning test divides into plurality the shift register which constitutes a scanning chain, and the way scanned for every divided shift register of this can be managed in a short time.

[0053] Although it had 3 sets of scanning test circuits of the gestalt of the 1st operation and the number of shift registers was made into six pieces as mentioned above with the gestalt of this operation, it is clear that this number's it can be set as arbitration with the usable number of terminals.

[0054]

[Effect of the Invention] As explained above, the scanning test circuit and the scanning test approach of this invention The 1st shift register which operates synchronizing with the 1st edge of a scanning clock, The 2nd shift register which operates synchronizing with the 2nd edge of the above-mentioned scanning clock, It has an output change means to change the 1st and 2nd scan-out data which is each output of the 1st and 2nd shift registers of the above, and to output scan-out result data. Since the shift register which constitutes two another scanning chains from the rising edge and falling edge of a scanning clock is operated If the number of terminals usable as a scanning in pin / a scan-out pin is equivalent, the number of scanning chains can be doubled substantially, therefore if the above-mentioned number of terminals and a clock frequency are equivalent, it is effective in the ability to reduce test time amount in one half.

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CLAIMS

[Claim(s)]
[Claim 1] It has the scanning chain which consists of series-connection circuits of two or more flip-flops for testing the internal circuitry of LSI which consists of a logical circuit, and is operated as a shift register. The scanning test data and the scanning clock for a test are inputted at the time of a static test mode. In the scanning test circuit which tests the scanning pass method which checks that carry out logical operation by said internal circuitry, and said internal circuitry is carrying out normal actuation based on the scan-out result data which are the output of the result of an operation Said 1st shift register which operates synchronizing with the 1st edge of said scanning clock, Said 2nd shift register which operates synchronizing with the 2nd edge of said scanning clock, The scanning test circuit characterized by having an output change means to change the 1st and 2nd scan-out data which is each output of said 1st and 2nd shift registers, and to output said scan-out result data.
[Claim 2] The scanning test circuit according to claim 1 characterized by for said 1st edge being a rising edge and said 2nd edge being a falling edge.
[Claim 3] The scanning test circuit according to claim 1 characterized by having the clock selector which answers supply of the inverter which reverses said scanning clock and outputs a reversal clock, and the scanning enable signal which activates a scanning test circuit at the time of said static test mode, chooses either of said scanning clocks and said reversal clocks, outputs a selection clock, and is supplied to said 2nd shift register.
[Claim 4] It has the scanning chain which consists of series-connection circuits of two or more flip-flops for testing the internal circuitry of LSI which consists of a logical circuit, and is operated as a shift register. The scanning test data and the scanning clock for a test are inputted at the time of a static test mode. In the scanning test circuit which tests the scanning pass method which checks that carry out logical operation by said internal circuitry, and said internal circuitry is carrying out normal actuation based on the scan-out result data which are the output of the result of an operation The scanning in pin which constitutes each of the 1st and 2nd scanning chains, and a scanning in signal inputs, The scanning clock pin which said scanning clock inputs, The 1st and 2nd shift registers which have the scan-out pin which outputs each of the scanning enabling pin [which the scanning enable signal which activates a scanning test circuit inputs], 1st, and 2nd scan-out signals at the time of said static test mode, respectively, The inverter which reverses said scanning clock and outputs a reversal clock, The selector for a clocked into change which answers supply of said scanning enable signal, chooses either of said scanning clocks and said reversal clocks at the time of said static test mode, outputs a selection clock, and is supplied to said scanning clock pin of said 2nd shift register, The scanning test circuit characterized by having the selector for an output change which chooses either of each and said 2nd scan-out signal of the 1st of said 1st and 2nd shift registers synchronizing with said scanning clock, and is outputted as said scan-out result data.
[Claim 5] When said scanning enable signal is the 1st level, said selector for a clocked into

change said scanning clock Said reversal clock is outputted as said selection clock, respectively at the time of the 2nd level. When said scanning clock is the 2nd level, said selector for an output change said 1st scan-out signal The scanning test circuit according to claim 4 characterized by outputting said 2nd scan-out signal as said scan-out result data, respectively at the time of the 1st level.

[Claim 6] n flip-flops with which each of said 1st and 2nd shift registers is the latch holding the data whose each is 1 bit, and constitutes the shift register of n (positive integer) bit, Said scanning clock is supplied as a shift clock of said flip-flop at the time of said internal circuitry of m (positive integer) individual for a scanning test, and the activity level of said scanning enable signal. The scanning test circuit according to claim 4 characterized by having a clock mask means to carry out the mask of said scanning clock at the time of non-activity level, and to suspend supply of said shift clock.

[Claim 7] The scanning test circuit according to claim 6 characterized by equipping said clock mask means with the AND circuit which outputs the AND of said scanning enable signal and said scanning clock.

[Claim 8] It has the scanning chain which consists of series-connection circuits of two or more flip-flops for testing the internal circuitry of LSI which consists of a logical circuit, and is operated as a shift register. At the time of a static test mode, the scanning test data and the scanning clock for a test are inputted. In the scanning test circuit which tests the scanning pass method which checks that carry out logical operation by said internal circuitry, and said internal circuitry is carrying out normal actuation based on the scan-out result data which are the output of the result of an operation The scanning in pin which constitutes each of the 1st and 2nd scanning chains, and the 1st scanning in signal inputs, The scanning clock pin which said scanning clock inputs, The 1st and 2nd shift registers which have the scan-out pin which outputs each of the scanning enabling pin [which the scanning enable signal which activates a scanning test circuit inputs], 1st, and 2nd scan-out signals at the time of a static test mode, respectively, The scanning in pin which constitutes each of the 3rd and 4th scanning chains, and the 2nd scanning in signal inputs, The scanning clock pin which said scanning clock inputs, The 3rd and 4th shift registers which have the scan-out pin which outputs each of the scanning enabling pin [which the scanning enable signal which activates a scanning test circuit inputs], 2nd, and 3rd scan-out signals at the time of said static test mode, respectively, The inverter which reverses said scanning clock and outputs a reversal clock, The selector for a clocked into change which answers supply of said scanning enable signal, chooses either of said scanning clocks and said reversal clocks at the time of said static test mode, outputs a selection clock, and is supplied to said scanning clock pin of said 2nd and 4th shift registers, The 1st selector for an output change which chooses either of each and said 2nd scan-out signal of the 1st of said 1st and 2nd shift registers synchronizing with said scanning clock, and is outputted as 1st scan-out result data, Synchronizing with said scanning clock, either of each and said 4th scan-out signal of the 3rd of said 3rd and 4th shift registers is chosen. The scanning test circuit characterized by having the 2nd selector for an output change outputted as 2nd scan-out result data.

[Claim 9] It has the scanning chain which consists of series-connection circuits of two or more flip-flops for testing the internal circuitry of LSI which consists of a logical circuit, and is operated as a shift register. The scanning test data and the scanning clock for a test are inputted at the time of a static test mode. In the test approach of a scanning pass method of checking carrying out logical operation by said internal circuitry, and said internal circuitry carrying out normal actuation based on the scan-out result data which are the output of the result of an operation Said 1st shift register is operated synchronizing with the 1st edge of said scanning clock. Said 2nd shift register is operated synchronizing with the 2nd edge of said scanning clock. The ** scan test approach characterized by changing the 1st and 2nd scan-out

data which is each output of said 1st and 2nd shift registers, and outputting said scan-out result data.

[Claim 10] The scanning test approach according to claim 9 characterized by for said 1st edge being a rising edge and said 2nd edge being a falling edge.

[Translation done.]

* NOTICES *

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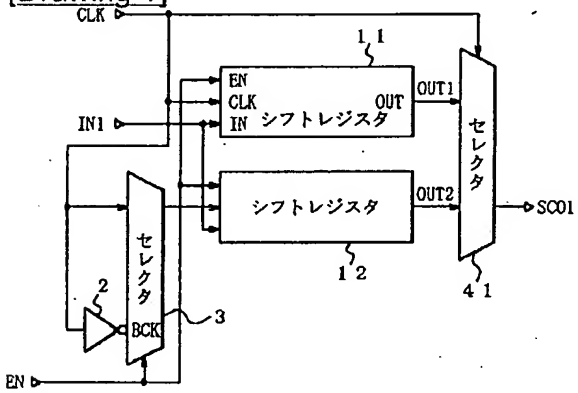
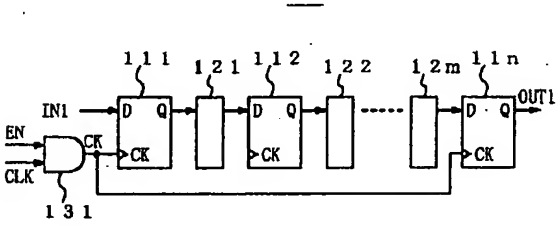
DRAWINGS

[Drawing 1]

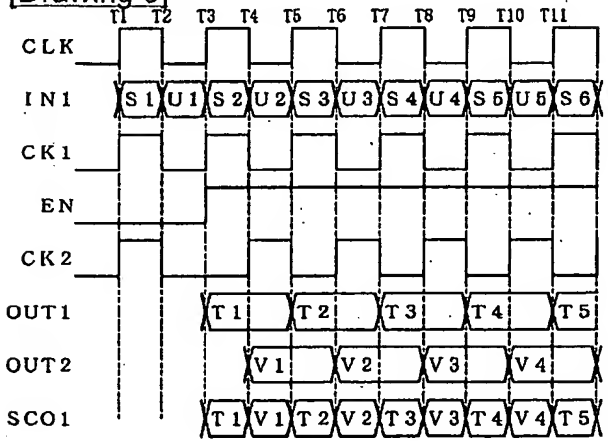


[Drawing 2]

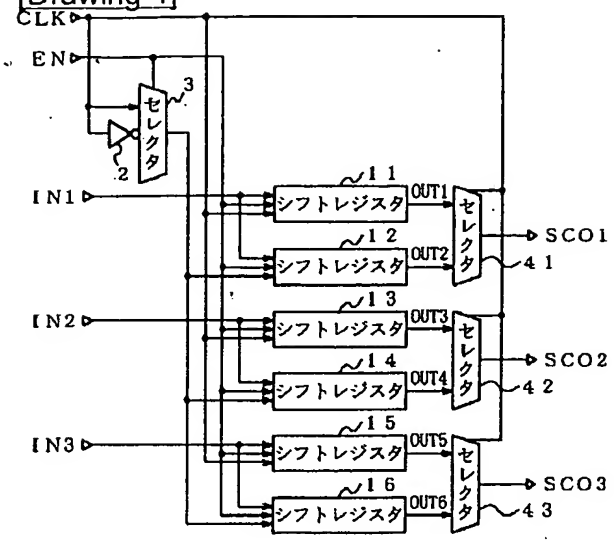


111, 112, ···, 11n : F/F
121, 122, ···, 12m : 内部回路

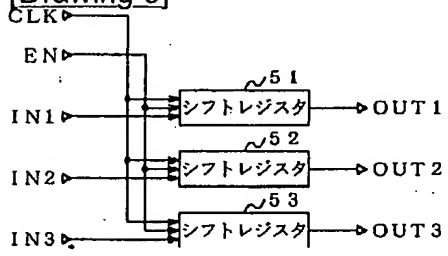
[Drawing 3]



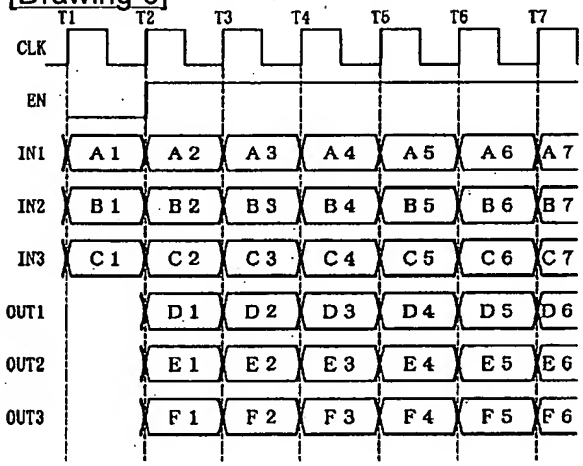
[Drawing 4]



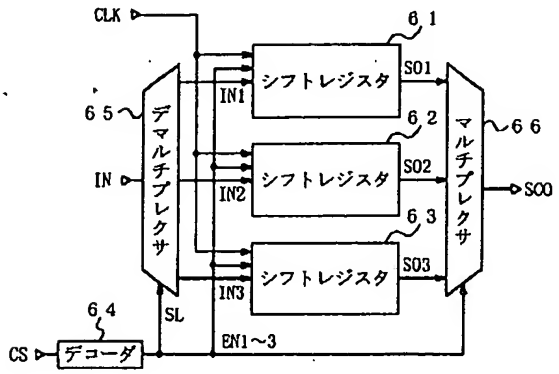
[Drawing 5]



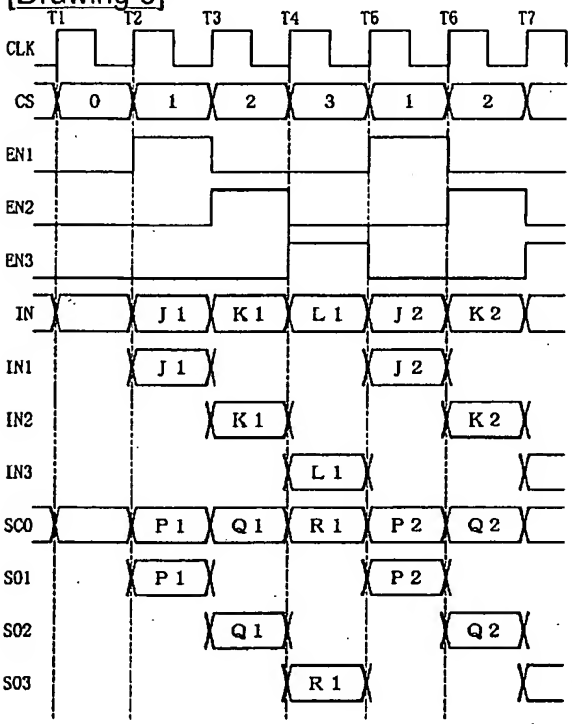
[Drawing 6]



[Drawing 7]



[Drawing 8]



[Translation done.]